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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,221	MICHELONI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 08 July 2005. The changes and remarks disclosed therein have been considered.

Claims 16-18 have been added by the Amendment. Therefore, claims 1-18 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 06 May 2005. The information disclosed therein was considered.

Specification

3. Claims 17 and 18 are objected to because of the following informalities:

Claim 17 recites "a compare block that inputs" which is different than "a compare block, this is input" recited in claim 8. Since claim 17 appears to be intended to include the subject matter of claim 8, said phrase in claim 17 will be understood as --a compare block, this is input--.

Claim 18 appears to be a duplicate of claim 15, since it appears to recite substantially the same elements in claim 15.

Appropriate correction is required.

Drawings

4. The replacement drawing sheets were received on 08 July 2005. The drawings on these replacement sheets are acceptable.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Mehrotra et al. (U.S. Pat. No. 5,659,550).

Mehrotra, for example in Figs. 4 and 6-12, discloses a method for erasing non-volatile memory cells in an integrated non-volatile memory device that comprises a memory cell array (40 in Fig. 4) organized in a row-and-column layout, and divided in array sectors (see, for example, Abstract), the method comprising: forcing an incompletely erased sector into a read condition (included in the combination test for determining the defective line type; see for example column 10, lines 11-18 and column 12, lines 27-40; see also column 3, lines 57-63 and column 4, lines 15-18) whenever the issue of the erase algorithm is incomplete or negative (whenever erase operations fail; see, for example, column 3, lines 12-26 and column 4, lines 43-48); scanning the rows of said sector to check the possible presence of a spurious current indicating a failed state (via, for example, 230 and/or 240 in Figs. 4, 6 and 7; see also column 4, lines 19-28), in a conduction path leading to a positive power (since positive voltages are used for various operations; see Fig. 3); identifying and electrically isolating the failed row (see, for

example, Abstract and column 4, lines 19-28); re-addressing from said failed row to a redundant row within a threshold distance of the failed row (if a word line is determined to be defective in the combination test; see for example column 4, lines 53-56); and re-starting the erase algorithm (to ensure that the re-addressed row is erased and not defective, to complete the erase operation).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrotra et al. (U.S. Pat. No. 5,659,550) in view of Horiguchi et al. (U.S. Pat. No. 5,262,993).

Regarding claim 4, Mehrotra discloses a method as in claim 1 above, with the exception of at least one switch provided between each one decode block and respective positive and negative power supplies in order to isolate the failed row.

Horiguchi '993, for example in Figs. 1, 4 and 5, discloses an EEPROM (see column 4, line 40) comprising at least one switch (for example, 141 and 142 in Figs. 4 and 5) provided between a memory block (including 20 and 21) and respective power supplies (VPL and VMP associated with the memory block) in order to isolate (or inhibit) a failed block (see for example column 2, lines 61-68). Horiguchi also discloses a short circuit type of failure (resulting in a spurious current) to which the disclosed means is applied (see for example column 2, lines 7-24).

Since it was common and well known in the art that, in an EEPROM, a positive and a negative voltages are provided to a word line via a word line driver within a row decoder, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the means of Horiguchi to the EEPROM of Mehrotra by providing a switch between the respective negative and positive supplies and the word line driver in order to isolate the failed row, for the purpose of providing a more reliable and robust means for repairing defects of a short circuit type (see for example Horiguchi '993, column 2, lines 7-24 and 44-68), thus increasing the life of such memory.

Regarding claim 6, the above Mehrotra/Horiguchi combination further discloses that said switches are driven by a logic (including 16 in Fig. 4 of Horiguchi '993) operatively interlinked to the contents of redundancy registers (for example, 35 in Fig. 2 of Horiguchi '993).

9. Claims 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrotra et al. in view of Horiguchi et al. (U.S. Pat. No. 5,265,055).

Mehrotra discloses a method as in claim 1, with the exception of said re-addressing being effected by means of a redundancy decode block incorporated inside the row decode circuitry; and the redundant row being adjacent or in the same sector as the sector containing the failed row.

Horiguchi '055 discloses an EEPROM (see for example column 7, lines 53-58) wherein re-addressing is effected by means of a redundancy decode block (for example, 600 in Fig. 9) incorporated inside a row decode circuitry (including 300 in Fig. 9); that a redundant row (for

example, within 120 in Fig. 9) is adjacent a same sector as the sector containing a failed row (if the regions 110 and 120 are interpreted as sectors; see column 8, lines 1-12) or in a same sector as the sector containing a failed row (if the mat 100 is interpreted as a sector; see column 8, lines 1-12).

Since an arrangement of redundant memory blocks near regular memory blocks was common and well known in the art (as exemplified in Horiguchi '055), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the redundant row of Mehrotra adjacent or in the same sector as the sector containing a failed row (as in Horiguchi '055, depending on how the sectors are defined), such that re-addressing is effected by a redundancy decode block inside a row decode circuitry (as in Horiguchi '055), for the purpose of effectively and efficiently repair/replace a defective row (see also Horiguchi '055, column 6, lines 59-65).

10. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USPN 5265055) in view of Horiguchi et al. (USPN 5262993).

Regarding claim 11, Horiguchi '055, for example in Fig. 9, discloses an integrated non-volatile memory device of the programmable and electrically erasable type (EEPROM; see column 7, line 58), comprising a memory cell array organized in a row-and-column layout (within 100-103), and divided in array sectors (100-103), each including at least one row decode circuit portion (for example, X DEC 300) being supplied positive and negative voltages (inherent in a word line decoder/driver for the EEPROM type), characterized in that it comprises: a

redundant row block (120) inside each sector (100); a plurality of row decode blocks (300 and 301) and at least one redundancy decode block (600) within the decode circuitry.

However, Horiguchi '055 does not disclose at least one switch between each one of the decode blocks and the respective positive and negative supplies in order to isolate a failed block during read, program or erase operations.

Horiguchi '993, for example in Figs. 1, 4 and 5, discloses an EEPROM (see column 4, line 40) comprising at least one switch (for example, 141 and 142 in Figs. 4 and 5) between a memory block (20) and respective power supplies (VPL and VMP associated with the memory block) in order to isolate (or inhibit) a failed block during read, program or erase operations (see for example column 2, lines 44-68).

Since it was common and well known in the art that, in an EEPROM, a positive and a negative voltages are provided to a word line via a word line driver within a row decoder, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the means of Horiguchi '993 to the EEPROM of Horiguchi '055 by providing a switch between the respective negative and positive supplies and the word line driver in order to isolate the failed row, for the purpose of providing a more reliable and robust means for repairing defects of a short circuit type (see for example Horiguchi '993, column 2, lines 7-24 and 44-68), thus increasing the life of such memory.

Regarding claims 12-14, the above Horiguchi/Horiguchi combination further discloses that said switches are MOS transistors (141 in Figs. 4 and 5 of Horiguchi '993); a control logic (including 16 in Fig. 4 of Horiguchi '993) for controlling said switches; that the operation of said

logic is interlinked with the contents of redundancy registers (for example, 35 in Fig. 2 of Horiguchi '993).

Allowable Subject Matter

11. The indicated allowability of claims 16-18 is withdrawn in view of the newly discovered reference(s) to Campardo et al. (U.S. Pat. No. 6,947,329). Rejections based on the newly cited reference(s) follow.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1-8 and 11-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,947,329 ("Patent"). Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claims 1-8, 16 and 17 of the instant application, claim 10 of Patent (together with parent claim 1) recites a method as in claim 1 of the instant application; and claims 2-8 of Patent recite substantially the same limitations as in claims 2-8, 16 and 17 of the instant application, since the subject matters of claims 7 and 8 (of the instant application) were incorporated into claims 16 and 17 (of the instant application), respectively, together with that of claim 1 (of the instant application).

However, claim 10 of Patent (together with parent claim 1) does not recite restarting the erase algorithm.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to restart the erase algorithm after re-addressing the failed row to a redundant row, for the purpose of ensuring that the re-addressed row is erased and not defective, and to complete the erase operation (see also claim 9 of Patent).

Regarding claims 11-15 and 18 of the instant application, claim 12 of Patent (together with parent claim 11) recites a device as in claims 11, 15 and 18 of the instant application.

Claim 12 of Patent (together with parent claim 11) is narrower in scope than claim 11 (of the instant application), since claim 12 of Patent (together with parent claim 11), for example, further recites "a compare block" not in claim 11 (of the instant application).

Similarly, claim 12 of Patent is narrower in scope than claims 15 and 18 (of the instant application), since claim 12 of Patent (together with parent claim 11), for example, further recites "isolating and relating to a redundant one even a single block having at least one row with a failed cell" not in claim 15 or 18 (of the instant application).

In addition, claims 13-15 of Patent recite substantially the same limitations as in claims 12-14.

Response to Arguments

14. Applicant's arguments on page 9 with respect to the rejection of claim 1 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of different application of the previously applied references. See rejections above.

15. Applicant's arguments regarding claim 11 have been fully considered but they are not persuasive.

Applicant argues, starting at the bottom of page 9, that "as evidenced by Figure 9 and other related figures, the redundancy decode block in Horiguchi '055 is not actually within the decode circuitry. The redundancy decode block in Horiguchi '055 is separate and apart from the decode circuitry. In Figure 9 and all other related figures, the spare word line selection circuit 600 is different and not within the Y-decoders 400 or the X-decoders 300-301 (see for example column 8, lines 5-8 and column 18, lines 16-1)."

In response, it is noted that "the decode circuitry" recited in claim 11 has been interpreted reasonably broadly to include all the decoding elements in the memory device; therefore, the spare word line selection circuit 600 with a decoding functionality in Fig. 9 of Horiguchi '055 would be "within the decoding circuitry" as recited in claim 11.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Griffus et al. (U.S. Pat. No. 5,502,674)

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER